REMARKS

Examiner Hung S. Bui is thanked for thoroughly reviewing the instant application and for examining the Prior Art.

Examiner is also thanked for the indication of allowing claims 6-17, 25-34, 40-51 and 59-68 if these claims are rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Favorable reconsideration of this application in light of the above amendments and the following remarks is respectfully requested.

A new method is provided for mounting a semiconductor on the surface of a Printed Circuit Board. A layer of Elastomer is deposited on the surface of the PCB, this layer of Elastomer makes the PCB into a thermally compliant PCB such that the thermal mismatch between the PCB and the semiconductor die that is mounted on the PCB is sharply reduced. Openings are created in the layer of Elastomer and electrical interfaces are created such that the PCB can be connected to the semiconductor die that is mounted on the PCB.

Claim rejections - 35 U.S.C. § 112

Reconsideration of the rejection of claims 52-56 and 71-72 under 35 U.S.C 112, second paragraph, being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention is respectfully requested based on the following arguments.

The Examiner is thanked for pointing out the various problems of insufficient structure in the claims. The claims have been carefully reviewed and amended to correct those problems the Examiner pointed out, in addition to others. All claims are now believed to be in allowable condition.

In light of the foregoing response, applicant respectfully requests that the Examiner's rejection of claims 52-56 and 71-72 under 35 U.S.C 112, second paragraph, be withdrawn.

Claim rejections - 35 U.S.C. § 103(a)

Reconsideration of the rejection of claims 1-5, 18-24, 35-39, 52-58 and 69-72 under 35 U.S.C 103(a) as being unpatentable over Anderson et al. (US Patent 5,969,461) in view of Lin et al. (US

Patent 5,450,283) is respectfully requested based on the following arguments.

Claim 1 has been amended by including allowable claim 6 and intervening claim 5 into claim 1.

Further, claim 35 has been amended by including allowable claim 40 into claim 35.

Since all the claims within this rejection are dependent upon amended claims 1 and 35 and carry all of the limitations of amended claims 1 and 35, applicant additionally asserts that those remaining claims may not also properly be rejected under 35 U.S.C 103(a) as being unpatentable over Anderson et al. (US Patent 5,969,461) in view of Lin et al. (US Patent 5,450,283), for reasons cited by the Examiner.

In light of the foregoing response, applicant respectfully requests that the Examiner's rejection of claims 1-5, 18-24, 35-39, 52-58 and 69-72 under 35 U.S.C 103(a), be withdrawn.

Other Considerations

No new independent or dependent claims have been written as a result of this office action, no new charges are therefore incurred due to this office action.

SUMMARY

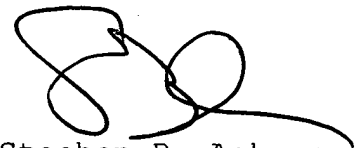
A new method is provided for mounting a semiconductor on the surface of a Printed Circuit Board. A layer of Elastomer is deposited on the surface of the PCB, this layer of Elastomer makes the PCB into a thermally compliant PCB such that the thermal mismatch between the PCB and the semiconductor die that is mounted on the PCB is sharply reduced. Openings are created in the layer of Elastomer and electrical interfaces are created such that the PCB can be connected to the semiconductor die that is mounted on the PCB.

It is requested that should Examiner not find the claims to be allowable that he call the undersigned Attorney at his convenience at 845-452-5863 to overcome any problems preventing allowance.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned:

"Version with markings to show changes made."

Respectfully submitted,



Stephen B. Ackerman (Reg. No 37,761)

Version with markings to show changes made

IN THE CLAIMS

Please amend the claims as follow:

1. (Amended) A method of providing thermal stress relieve for packages [that are] used for [the] mounting [of] semiconductor devices, comprising [the] steps of:

providing a circuit board [on the surface of which] having at least one point of electrical contact [has been provided];

forming one or more layers of thermal stress relieve material on [the surface of] said circuit board;

providing one or more semiconductor devices for mounting on said circuit board, said one or more semiconductor devices having been provided with points of electrical contact; and

establishing electrical contact between said at least one point of electrical contact provided [in the surface of] on said circuit board and said points of electrical contact provided in said semiconductor devices, said establishing electrical contact between said at least one point of electrical contact provided on said circuit board and said points of electrical contact provided in said semiconductor devices comprising Printed

Circuit Board technology or Build Up Board technology, said Printed Circuit Board technology comprising:

(i) creating one or more openings in said created layers of thermal stress relieve material whereby said one or more openings align with one or more overlying points of electrical contact on one or more created layers of said thermal stress relieve material;

(ii) depositing a layer of conductive material over said created layers of thermal stress relieve material, including said openings; and

(iii) patterning said layer of conductive material, forming a upper layer of interconnect lines and contact pads on said created one or more layers of said thermal stress relieve material, exposing the surface of said thermal stress relieve material.

2. (Amended) The method of claim 1, [wherein] said semiconductor devices [are] being flip chip devices [whereby said flip chip devices have] having been provided with solder bumps [for electrical interconnect of said flip chips with surrounding electrical circuitry or components].

5. Please cancel claim 5.

6. Please cancel claim 6.

7. (Amended) The method of claim [6] 1 wherein said creating one or more openings in said created layers of thermal stress relieve material comprises methods of photolithography.

8. (Amended) The method of claim [6] 1 wherein said depositing a layer of conductive material over said created layers of thermal stress relieve material comprises steps of electroless seeding followed by electroplating of [the surface of] said created layers of said thermal stress relieve material.

9. (Amended) The method of claim [6] 1 with [the] additional steps of:

depositing a layer of dielectric over said upper layer of interconnect lines, including [the surface of] said [partially] exposed thermal stress relieve material;

depositing a solder mask over said layer of dielectric; and

patterning said layer of dielectric, [to open] exposing an array of conductive pads in the layer of dielectric, said conductive pads having been connected to at least one of said at least one point [points] of electrical contact provided on [the surface of] said circuit board, said conductive pads further

being points of electrical contact for said one or more semiconductor devices.

10. (Amended) The method of claim 9 with [the] additional steps of:

positioning said semiconductor devices above said circuit board, [such that] said array of conductive pads in the layer of dielectric [aligns] being aligned and [is] in contact with said points of electrical contact of said semiconductor devices; and

connecting said array of conductive pads in the layer of dielectric with said points of electrical contact for said semiconductor devices by [methods of] thermal reflow [or any other method to connect points of electrical contact for said semiconductor devices with said array of conductive pads].

11. (Amended) The method of claim [5] 1 wherein said [methods of] Build Up Board technology [for establishing electrical contact between overlying points of electrical contact is] comprises interconnecting a first pattern of interconnect lines and contact pads to a second pattern of interconnect lines and contact pads, said first pattern of interconnect lines and contact pads being created on an underlying or first layer of thermal stress relieve material, comprising [the] steps of:

depositing a first layer of conductive material on [the surface of said underlying] a first layer of [created layer of] thermal stress relieve material;

[pattering] patterning [and etching] said first layer of conductive material, creating a first pattern of interconnect lines or contact pads;

creating a second layer of thermal stress relieve material on [the surface of] said [underlying] first layer of thermal stress relieve material including said first pattern of interconnect lines or contact pads;

creating vias in said second layer of stress relieve material, said vias overlying interconnect lines or contact pads of said first pattern [to which said electrical contact is to be established];

depositing a second layer of conductive material on [the surface of] said second layer of stress relieve material, including said vias, connecting said second layer of conductive material to said first pattern of interconnect lines or contact pads; and

[pattering] patterning [and etching] said second layer of conductive material, creating a second pattern of interconnect lines or contact pads, [partially] exposing [the surface of] said created second layer of thermal stress relieve material.

13. (Amended) The method of claim 11, [wherein] said [methods of] Build Up Board technology [for establishing electrical contact between overlying points of electrical contact is] being applied one or more times during said step of creating a layer of thermal stress relieve material on [the surface of] said circuit board, creating multiple overlying vias [that interconnect] interconnecting multiple layers of interconnect lines and contact pads.

14. (Amended) The method of claim 11 wherein said depositing a first layer of conductive material comprises steps of electroless seeding followed by electroplating of [the surface of] said [underlying] first layer of said thermal stress relieve material.

15. (Amended) The method of claim 11 wherein said depositing a second layer of conductive material comprises steps of electroless seeding followed by electroplating of [the surface of] said created second layer of said thermal stress relieve material, said step of electroless seeding followed by electroplating [to be] being performed after said creation of vias in said [created] second layer of thermal stress relieve material.

16. (Amended) The method of claim 11 with [the] additional steps of:

depositing a layer of dielectric over said second layer of conductive material, including [the surface of] said [partially] exposed second layer of thermal stress relieve material;

depositing a solder mask over said layer of dielectric; and

patterning said layer of dielectric, [to open] exposing an array of conductive pads in the layer of dielectric, said conductive pads having been connected to at least one of said points of electrical contact provided on [the surface of] said circuit board, said conductive pads further being points of electrical contact for said one or more semiconductor devices.

17. (Amended) The method of claim 16 with [the] additional steps of:

positioning said semiconductor devices above said circuit board, [such that] said array of conductive pads [in the layer of dielectric] of said second pattern of interconnect lines or contact pads [aligns and is] being aligned and in contact with said points of electrical contact of said semiconductor devices; and

connecting said array of conductive pads [in the layer of dielectric] of said second pattern of interconnect lines or contact pads with said points of electrical contact for said

semiconductor devices by [methods of] thermal reflow [or any other method to connect points of electrical contact for said semiconductor devices with said array of conductive pads].

18. (Amended) The method of claim 1 with [the] an additional step of [treating] etching or swelling one or more of said created layers of thermal stress relieve material [by methods of etching or swelling], thereby roughening [to roughen the surface of] said created layers, [and thereby promote] enhancing adhesion for a subsequent electroless metal deposition, said additional step [to be] being performed after said step of creating a layer of thermal stress relieve material.

19. (Amended) The method of claim 1 with [the] an additional step of curing one or more of said created layers of thermal stress relieve material, said additional step [to be] being performed after said step of creating a layer of thermal stress relieve material.

20. (Amended) The method of claim 19 wherein said curing [is] comprises thermal curing technology.

21. (Amended) The method of claim 19 wherein said curing [is] comprises E-beam curing technology.

22. (Amended) The method of claim 19 wherein said curing [is] comprises UV curing technology.

23. (Amended) The method of claim 1 wherein establishing electrical contact between said at least one point of electrical contact provided [in the surface of] on said circuit board and said points of electrical contact provided in said semiconductor devices is providing contact pads on [the surface of] said created layers of thermal stress relieve material, said contact pads having been connected to at least one of said points of electrical contact provided on [the surface of] said circuit board, said contact pads further being points of electrical contact for said semiconductor devices.

24. (Amended) The method of claim 1 wherein establishing electrical contact between said at least one point of electrical contact provided [in the surface of] on said circuit board and said points of electrical contact provided in said semiconductor devices is providing at least one conducting interconnect through said created layers of thermal stress relieve material, said conducting interconnects having been connected to at least one of said points of electrical contact provided on [the surface of] said circuit board using [interconnect methods of]

PCB technology or Build Up Board technology, said conducting interconnects further being points of electrical contact for said semiconductor devices.

25. (Amended) The method of claim 1 wherein establishing electrical contact between said at least one point of electrical contact provided [in the surface of] on said circuit board and said points of electrical contact provided in said semiconductor devices is providing at least one contact pad on [the surface of] said [created] layers of thermal stress relieve material in addition to providing at least one conducting interconnect through said [created] layers of thermal stress relieve material, said contact pads on [the surface of] said [created] layers of thermal stress relieve material having been connected to at least one of said conducting interconnect through said [created] layers of thermal stress relieve material, said conducting interconnects having been connected to at least one of said points of electrical contact points provided on [the surface of] said circuit board using [interconnect methods of] PCB technology or Build Up Board technology, said contact pads on [the surface of] said [created] layers of thermal stress relieve material being points of electrical contact for said semiconductor devices.

26. (Amended) The method of claim 25 wherein providing at least one contact pad on [the surface of] said created layers of thermal stress relieve material comprises [the] steps of:

depositing a layer of conducting material over [the surface of] said created layer of thermal stress relieve material;

patterning [and etching] said layer of conducting material, creating a pattern of interconnect lines on [the surface of] said created layer of thermal stress relieve material, [partially] exposing said thermal stress relieve material;

depositing a layer of dielectric over [the surface of] said pattern of interconnect lines, including [the surface of] said [partially] exposed thermal stress relieve material;

depositing a solder mask over said layer of dielectric; and

patterning said layer of dielectric, [to open] exposing an array of conductive pads in the layer of dielectric, said conductive pads having been connected to at least one of said points of electrical contact provided on [the surface of] said circuit board, said conductive pads further being points of electrical contact for said semiconductor devices.

27. (Amended) The method of claim 26 with [the] additional steps of:

positioning said semiconductor devices above said circuit board, [such that] said array of conductive pads in the layer of

dielectric [aligns] being aligned and [is] in contact with said points of electrical contact of said semiconductor devices; and

connecting said array of conductive pads in the layer of dielectric with said points of electrical contact for said semiconductor devices by [methods of] thermal reflow [or any other method to connect points of electrical contact for said semiconductor devices with said array of conductive pads].

28. (Amended) The method of claim [5] 1 wherein said [methods of] Build Up Board technology [for establishing electrical contact between overlying points of electrical contact] is interconnecting a first pattern of interconnect lines and contact pads to a second pattern of interconnect lines and contact pads, said first pattern of interconnect lines and contact pads being created on a BGA surface, comprising [the] steps of:

providing a semiconductor surface having been provided with points of electrical contact [in its surface];

creating a layer of thermal stress relieve material on [the surface of] said semiconductor surface;

creating vias in said layer of stress relieve material, said vias overlying said points of electrical contact provided in [the surface of] said semiconductor surface;

depositing a layer of conductive material on [the surface of] said layer of stress relieve material, including said vias, connecting said layer of conductive material to points of electrical contact provided in said semiconductor surface; and

[pattering] patterning [and etching] said layer of conductive material, creating a pattern of interconnect lines or contact pads, [partially] exposing [the surface of] said created layer of thermal stress relieve material.

29. The method of claim 28 wherein said semiconductor surface is the surface of a BGA substrate.

30. The method of claim 28 wherein said creation of vias comprises methods of lithographic etching or laser drilling.

31. (Amended) The method of claim 28 wherein said [methods of] Build Up Board technology [for establishing electrical contact between overlying points of electrical contact] is applied one time during said step of creating a layer of thermal stress relieve material on [the surface of] said semiconductor surface, creating a first [created] layer of thermal stress relieve material on said semiconductor surface.

32. (Amended) The method of claim 28 wherein said depositing a layer of conductive material comprises steps of electroless seeding followed by electroplating of [the surface of] said underlying layer of said thermal stress relieve material, said steps of electroless seeding followed by electroplating [to be] being performed after said creation of vias in said created layer of thermal stress relieve material.

33. (Amended) The method of claim 28 with [the] additional steps of:

depositing a layer of dielectric over said pattered layer of conductive material, including [the surface of] said [partially] exposed thermal stress relieve material;

depositing a solder mask over said layer of dielectric; and

patterning said layer of dielectric, exposing [to open] an array of conductive pads in the layer of dielectric, said conductive pads having been connected to at least one of said points of electrical contact provided on [the surface of] said circuit board, said conductive pads further being points of electrical contact for said semiconductor devices.

34. (Amended) The method of claim 33 with [the] additional steps of:

positioning said semiconductor devices above said circuit board, [such that] said array of conductive pads in the layer of dielectric [aligns] being aligned and [is] in contact with said points of electrical contact of said semiconductor devices; and

connecting said array of conductive pads in the layer of dielectric with said points of electrical contact for said semiconductor devices by [methods of] thermal reflow [or any other method to connect points of electrical contact for said semiconductor devices with said array of conductive pads].

35. (Amended) A structure for providing thermal stress relieve for packages that are used for the mounting of semiconductor devices, comprising:

a circuit board on [the surface of] which at least one point of electrical contact has been provided;

one or more layers of thermal stress relieve material created on [the surface of] said circuit board;

one or more semiconductor devices for mounting on said circuit board, said semiconductor devices having been provided with points of electrical contact; and

electrical contact between said point of electrical contact provided [in the surface of] on said circuit board and said points of electrical contact provided in said semiconductor devices, said electrical contact having been established using

Printed Circuit Board technology or Build Up Board technology, said Printer Board technology comprising creating one or more openings in said one or more layers of thermal stress relieve material aligned with said at least one point of electrical contact provided on said circuit board, by depositing a layer of conductive material over said created layers of thermal stress relieve material, including said one or more openings and by creating an upper layer of interconnect lines and contact pads formed by patterning said layer of conductive material on said layer of said thermal stress relieve material.

36. (Amended) The structure of claim 35, [wherein] said semiconductor devices [are] being flip chip devices [whereby said flip chip devices have] having been provided with solder bumps [for electrical interconnect of said flip chips with surrounding electrical circuitry or components].

39. Please cancel clam 39.

40. Please cancel claim 40.

41. Please cancel claim 41.

42. Please cancel claim 42.

43. (Amended) The structure of claim [40] 35, additionally comprising [with the addition of]:

a layer of dielectric deposited over said upper layer of interconnect lines, including [the surface of] said [partially] exposed thermal stress relieve material;

a solder mask deposited over said layer of dielectric; and

an array of conductive pads in the layer of dielectric created by patterning said layer of dielectric, said conductive pads having been connected to at least one of said points of electrical contact provided on [the surface of] said circuit board, said conductive pads further being points of electrical contact for said semiconductor devices.

44. (Amended) The structure of claim 43, [with the addition of] additionally comprising:

[positioning] said semiconductor devices having been positioned above said circuit board such that said array of conductive pads in the layer of dielectric aligns and is in contact with said points of electrical contact of said semiconductor devices; and

[connecting] said array of conductive pads in the layer of dielectric having been connected with said points of electrical contact for said semiconductor devices [by methods of thermal

reflow or any other method to connect points of electrical contact for said semiconductor devices with said array of conductive pads].

45. (Amended) The structure of claim [39] 35 wherein said [methods of] Build Up Board technology [for establishing electrical contact between overlying points of electrical contact is] comprises interconnecting a first pattern of interconnect lines and contact pads to a second pattern of interconnect lines and contact pads, said first pattern of interconnect lines and contact pads having being created on [an underlying] a first layer of thermal stress relieve material, said second pattern of interconnect lines and contact pads having been created on a second layer of thermal stress relieve material[, comprising the steps of:

depositing a first layer of conductive material on the surface of said underlying layer of created layer of thermal stress relieve material;

pattering and etching said first layer of conductive material, creating a first pattern of interconnect lines or contact pads;

creating a layer of thermal stress relieve material on the surface of said underlying layer of thermal stress relieve

material including said first pattern of interconnect lines or contact pads;

creating vias in said layer of stress relieve material, said vias overlying interconnect lines or contact pads to which said electrical contact is to be established;

depositing a second layer of conductive material on the surface of said layer of stress relieve material, including said vias, connecting said second layer of conductive material to said first pattern of interconnect lines or contact pads; and

pattering and etching said second layer of conductive material, creating a second pattern of interconnect lines or contact pads partially exposing the surface of said created layer of thermal stress relieve material].

46. Please cancel claim 46.

47. (Amended) The structure of claim 45, [wherein] said [methods of] Build Up Board technology [for establishing electrical contact between overlying points of electrical contact is] having been applied one or more times during [said step of] creating a layer of thermal stress relieve material on [the surface of] said circuit board, [creating] having created multiple overlying vias [that interconnect] interconnecting multiple layers of interconnect lines and contact pads.

48. Please cancel claim 48.

49. Please cancel claim 49.

50. (Amended) The structure of claim 45, additionally comprising [with the addition of]:

a layer of dielectric deposited over said second layer of conductive material, including [the surface of] said [partially exposed] second layer of thermal stress relieve material;

a solder mask deposited over said layer of dielectric; and

an array of conductive pads in the layer of dielectric having been created by patterning said layer of dielectric, said conductive pads having been connected to at least one of said points of electrical contact provided on [the surface of] said circuit board, said conductive pads further being points of electrical contact for said one or more semiconductor devices.

51. (Amended) The structure of claim 50, additionally comprising [with the addition of]:

[positioning] said semiconductor devices having been positioned above said circuit board such that said array of conductive pads in the layer of dielectric aligns and is in

contact with said points of electrical contact of said semiconductor devices; and

[connecting] said array of conductive pads in the layer of dielectric having been connected with said points of electrical contact for said semiconductor devices [by methods of thermal reflow or any other method to connect points of electrical contact for said semiconductor devices with said array of conductive pads].

52. (Amended) The structure of claim 35 with [the addition] additionally [of treating] comprising etching or swelling one or more of said created layers of thermal stress relieve material [by methods of etching or swelling], thereby having roughened [to roughen] [the surface of] said created layers and thereby [promote] enhancing adhesion for a subsequent electroless metal deposition [said additional step to be performed after said step of creating a layer of thermal stress relieve material].

53. (Amended) The structure of claim 35 with [the addition] additionally [of curing] said one or more [of said created] layers of thermal stress relieve material having been cured [said additional step to be performed after said step of creating a layer of thermal stress relieve material].

54. Please cancel claim 54.

55. Please cancel claim 55.

56. Please cancel claim 56.

57. (Amended) The structure of claim 35, [wherein] electrical contact between said point of electrical contact provided in [the surface of] said circuit board and said points of electrical contact provided in said semiconductor devices [is] having been established by providing contact pads on [the surface of] said created layers of thermal stress relieve material, said contact pads having been connected to at least one of said points of electrical contact provided on [the surface of] said circuit board, said contact pads further being points of electrical contact for said semiconductor devices.

58. (Amended) The structure of claim 35, [wherein] electrical contact between said point of electrical contact provided in [the surface of] said circuit board and said points of electrical contact provided in said semiconductor devices [is] having been established by providing at least one conducting interconnect through said created layers of thermal stress relieve material, said conducting interconnects having been

connected to at least one of said points of electrical contact provided on [the surface of] said circuit board using interconnect methods of PCB technology or Build Up Board technology, said conducting interconnects further being points of electrical contact for said semiconductor devices.

59. (Amended) The structure of claim 35, [wherein] electrical contact between said point of electrical contact provided in [the surface of] said circuit board and said points of electrical contact provided in said semiconductor devices [is] having been established by providing at least one contact pad on [the surface of] said created layers of thermal stress relieve material in addition to [providing] having provided at least one conducting interconnect through said created layers of thermal stress relieve material, said contact pads on [the surface of] said created layers of thermal stress relieve material having been connected to said at least one [of said] conducting interconnect through said created layers of thermal stress relieve material, said conducting interconnects having been connected to at least one of said points of electrical contact points provided on [the surface of] said circuit board [using interconnect methods of PCB technology or Build Up Board technology], said contact pads on [the surface of] said created

layers of thermal stress relieve material being points of electrical contact for said semiconductor devices.

60. (Amended) The structure of claim 59 wherein at least one contact pad on [the surface of] said created layers of thermal stress relieve material comprises [is provided comprising the steps of]:

[depositing] a patterned layer of conducting material over [the surface of] said created layer of thermal stress relieve material, [;]

[patterning and etching said layer of conducting material, creating] comprising a pattern of interconnect lines on [the surface of] said created layer of thermal stress relieve material[, partially exposing said thermal stress relieve material];

[depositing] a layer of dielectric deposited over [the surface of] said pattern of interconnect lines[, including the surface of said partially exposed thermal stress relieve material];

[depositing] a solder mask deposited over said layer of dielectric; and

[patterning] said layer of dielectric having been patterned, [to open] exposing an array of conductive pads in the layer of dielectric, said conductive pads having been connected

to at least one of said points of electrical contact provided on [the surface of] said circuit board, said conductive pads further being points of electrical contact for said semiconductor devices.

61. (Amended) The structure of claim 60, additionally comprising [with the addition of]:

[positioning] said semiconductor devices having been positioned above said circuit board such that said array of conductive pads in the layer of dielectric aligns and is in contact with said points of electrical contact of said semiconductor devices; and

[connecting] said array of conductive pads in the layer of dielectric having been connected with said points of electrical contact for said semiconductor devices [by methods of thermal reflow or any other method to connect points of electrical contact for said semiconductor devices with said array of conductive pads].

62. (Amended) The structure of claim 39 wherein said [methods of] Build Up Board technology [for establishing electrical contact between overlying points of electrical contact is] comprises interconnecting a first pattern of interconnect lines and contact pads to a second pattern of interconnect lines and

contact pads, said first pattern of interconnect lines and contact pads being created on a BGA surface, comprising [the steps of]:

[providing] a semiconductor surface having been provided with points of electrical contact in its surface;

[creating] a layer of thermal stress relieve material having been created on [the surface of] said semiconductor surface;

[creating] vias having been created in said layer of stress relieve material, said vias overlying said points of electrical contact provided in [the surface of] said semiconductor surface;

[depositing] a layer of conductive material having been deposited on [the surface of] said layer of stress relieve material, including said vias, connecting said layer of conductive material to electrical contact provided in said semiconductor surface; and

[pattering and etching] said layer of conductive material having been patterned, having created [creating] a pattern of interconnect lines or contact pads, [partially] exposing [the surface of] said created layer of thermal stress relieve material.

64. Please cancel claim 64.

65. (Amended) The structure of claim 62, [wherein] said [methods of] Build Up Board technology [for establishing electrical contact between overlying points of electrical contact is] having been applied one time during said step of creating a layer of thermal stress relieve material on [the surface of] said semiconductor surface, [creating] having created a first created layer of thermal stress relieve material on said semiconductor surface.

66. Please cancel claim 66.

67. (Amended) The structure of claim [66] 62, additionally comprising [with the addition of]:

a layer of dielectric deposited over said pattered layer of conductive material, including [the surface of] said [partially] exposed thermal stress relieve material;

a solder mask deposited over said layer of dielectric; and

an array of conductive pads in the layer of dielectric created by patterning said layer of dielectric, said conductive pads having been connected to at least one of said points of electrical contact provided on [the surface of] said circuit board, said conductive pads further being points of electrical contact for said semiconductor devices.

68. (Amended) The structure of claim 67, additionally comprising [with the addition of]:

[positioning] said semiconductor devices having been positioned above said circuit board such that said array of conductive pads in the layer of dielectric aligns and is in contact with said points of electrical contact of said semiconductor devices; and

[connecting] said array of conductive pads in the layer of dielectric having been connected with said points of electrical contact for said semiconductor devices [by methods of thermal reflow or any other method to connect points of electrical contact for said semiconductor devices with said array of conductive pads].

69. Please cancel claim 69.

70. Please cancel claim 70.

71. Please cancel claim 71.

73. Please cancel claim 73.